

ABSTRACT OF THE DISCLOSURE

In a display device using a time gradation method, electric power consumption at a time when high-level gradation display is unnecessary is reduced. Writing of a digital video signal of a lower order bit into a memory is eliminated by a memory controller of a signal control circuit in a display device, during a second display mode in which the number of gradations is reduced as compared to in a first display mode of high-level gradation. In addition, read out of the digital video signal of the lower order bit from the memory is also eliminated. The amount of information of a digital image signal inputted to a source signal line driver circuit is reduced. In accordance with such operation, a display controller functions to make start pulses and clock pulses inputted to the source signal line driver circuit have a lower frequency and to lower a driving voltage. When the gradation is reduced, a frame period in the second display mode may be set longer as compared to that in the first display mode, and therefore low electric power consumption is achieved.